Sierra 1914B

DATA TRANSMISSION TEST SET

OPERATION MANUAL

PHILCO Ford

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NOTICE
TO THE PURCHASER OF
THE SIERRA 1914B DATA TRANSMISSION TEST SET

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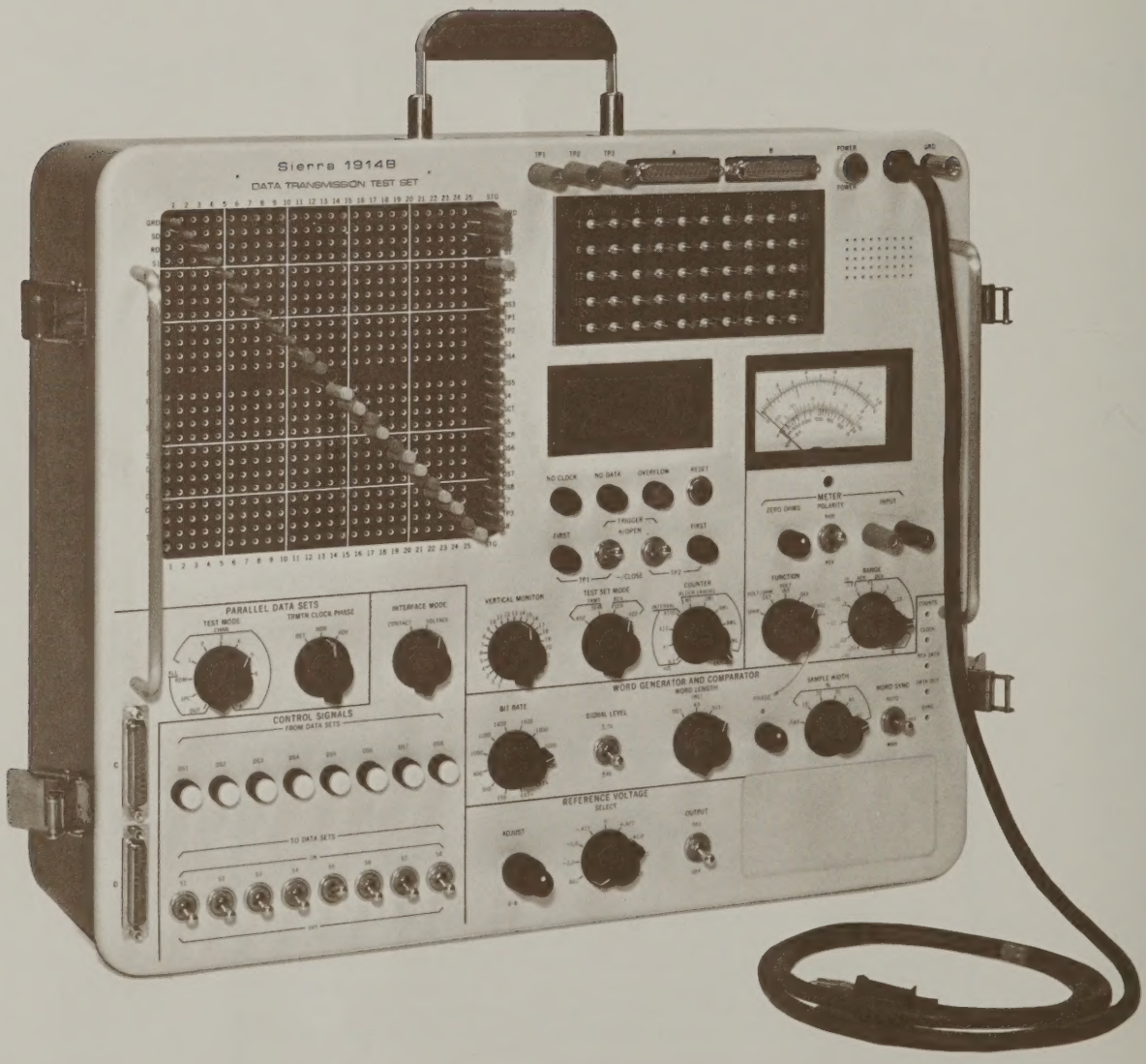

Figure 1. Sierra 1914B Data Transmission Test Set

1914B DATA TRANSMISSION TEST SET DESCRIPTION AND OPERATION

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1. GENERAL

1.01 This manual provides a physical and functional description of the Sierra 1914B Data Transmission Test Set and presents the operation theory required for effective use of the instrument.

1.02 The Sierra 1914B Data Transmission Test Set is a portable instrument for tests of voiceband data systems. It is compatible with digital and analog modems now in operation and contains built-in flexibility to allow its use on future systems. Either synchronous or asynchronous serial-data modems can be tested. For tests of asynchronous modems, an internal clock produces test messages at any of ten bit rates selected. Synchronous-data modems that recover their own clock signals can be tested at any bit rate in the range of 10 to 20,000 bits per second, as determined by modem characteristics. Two detectors and associated lamps provide a visual indication of a failure of the clock signal and a failure of the data signal. Control signals applied to the interface of the modem are generated by individual switches. Control signals from the modem are readily monitored by indicator lamps.

1.03 The 1914B can be used at both the transmitting and receiving station of a data system. A major advantage of the 1914B is its programmable crosspoint matrix, which establishes the connection of the internal test circuits to the interface leads of the data modem. This matrix provides total flexibility in all interface interconnections and, together with an array of interface switches, permits tests of a modem or data system while the data terminal is connected to the transmitting or receiving modem.

1.04 The performance of the data transmission system is evaluated in terms of the bit or block error rate of the system. The errors are tabulated and displayed on an electronic decade counter. In block error tests the block length can be adjusted from a minimum of 63 to a maximum in excess of 8000 bits. In tests of asynchronous modems the received data signal is sampled at the mid-bit position by a pulse which is adjustable in width. This feature permits determining in one test the error rate of the system and also the margin against errors.

1.05 Features of the 1914B are:

- Full compatibility with most voice-frequency modems
- Performs dynamic and static tests of data transmission systems
- Tests both asynchronous and synchronous serial modems as well as eight-channel parallel modems
- Bit and block error counting
- Three types of digital test messages – dot signal, 63-bit, and 511-bit pseudorandom word
- Checks sequence of control signals and measures time intervals
- Provides internally clocked bit rates for tests of asynchronous modems in the range of 150 to 2400 bits per second
- Can be operated from clock signal of synchronous modems at bit rates in the range of 10 to 20,000 bits per second.

- Automatic and manual word synchronization
- Variable-width sample window for receive data bits to permit determining error rate margins
- Internal dc voltmeter for checks of dc interface voltages
- High-impedance ac voltmeter and loudspeaker amplifier for monitoring line signals
- Interface signals conform to EIA specification RS 232B and CCITT recommendations
- Compatible with Bell System 902-903 series test sets
- Equivalent to Western Electric Company Model 914B data test set.

2. PHYSICAL DESCRIPTION

2.01 The 1914B Data Transmission Test Set is contained in a carrying case measuring approximately 18-1/2 inches in width, 15 inches in height, and 7-1/2 inches in depth. It weighs about 27 pounds. Figure 1 shows the 1914B ready for use, Figure 2 shows the test set with its cover in place, and Figure 3 is a view of the inside of the cover showing the two interface connector cables, the two test leads, and the 4-dB attenuator.

Figure 2. Sierra 1914B with Cover in Place

2.02 The test set is powered by a self-contained power supply which draws approximately 60 watts of 105- to 125-volt, 48- to 65-Hz commercial power. It will operate efficiently in an environment with an ambient temperature ranging from +40° to +120°F and a relative humidity of from 20 to 95 percent.

2.03 Figures 4 and 5 show the front panel of the 1914B. The program matrix in the upper left-hand corner provides access to the interface leads of the data set being tested. The 25 vertical buses connect to the interface leads and the 24 horizontal buses connect to the test circuits provided by the 1914B. Connections from the input or output leads of the test circuits to the interface leads are made by inserting program pins at the intersections of the appropriate vertical and horizontal buses of the matrix. The meanings of the designations stamped alongside the buses are given in the following tabulation.

1914B Designation	EIA RS232B or C Designation	CCITT V-24 Designation	Meaning
GRD	AA, AB	101, 102	Ground
SD	BA	103	Send Data, Output
RD	BB	104	Receive Data, Input
SCT	DB	114	Serial Clock Transmit, Input
SCR	DD	115	Serial Clock Receive, Input
DS1-DS8			Inputs to Lamps DS1-DS8
S1-S8			Outputs from S1-S8
TP1-TP3			Test Point Connections
STG			Program Pin Storage

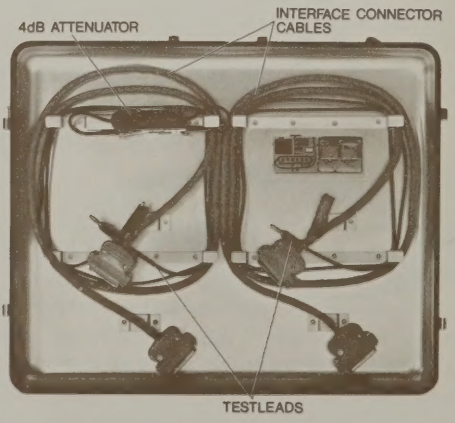


Figure 3. Inside Front Cover

2.04 The interface leads connect through push-pull selector switches on the front panel (Figure 4) to the vertical buses of the program matrix. These switches permit testing a data set on an in-service basis in either a bridging or terminating mode. They also offer a means of testing data sets having more than 25 interface leads.

2.05 The other front-panel controls, indicators, and connectors are described in Table 1. Abbreviations marked on some of the switch positions are defined as follows:

Designation	Meaning
CHAN	Parallel Data Channel
ALL RDM	Random Test Signal on All Channels
ALL SPC	Spacing Signal on All Channels
ALL DOT	Dot Signal on All Channels
SER	Serial
WL, 2WL, etc.	Word Length; Block Length in Multiples of the Word Length (63 or 511) Selected
AUTO	Automatic
MAN	Manual

Table 1. Front-Panel Controls, Indicators, and Connectors

KEY	DEVICE	FUNCTION
1	Program Matrix	Provides access to the interface leads of the data set being tested
2	Interface selector switches	Provide access to the interface leads for in-service testing of data sets.
3	TP1 and TP2 test points	Provide means of introducing signals into the interval counter. Also provide access to TP1 and TP2 matrix buses.
4	TP3 test point	Provides access to the TP3 matrix bus and the selected reference voltage, when the REFERENCE VOLTAGE OUTPUT switch is in the TP3 position.
5	Connector A	Provides connection to serial data set interface.
6	Connector B	Provides connection to business machine interface for in-service tests of serial data sets.
7	POWER switch and lamp	Provides means of turning set on and off and provides power on indication.
8	GRD connector	Provides means of connecting an external ground.
9	Loudspeaker	Permits the operator to audibly monitor signals on any line connected to the METER INPUT terminals when the FUNCTION switch is in the SPKR position.
10	Counter display	Provides a two-digit readout of error count or interval, depending on the position of the COUNTER switch.

Table 1. Front-Panel Controls, Indicators, and Connectors (Cont)

KEY	DEVICE	FUNCTION
11	METER	Indicates ac voltage, dc voltage, or resistance, depending on the setting of the FUNCTION and RANGE switches.
12	OVERFLOW lamp	When lighted, indicates counter capacity has been exceeded.
13	RESET switch	Clears counter and resets interval test circuits.
14	FIRST TP2 lamp	When lighted, indicates preselected signal appeared first on TP2 lead.
15	ZERO OHMS adjustment	Provides a means of calibrating the ohmmeter for zero ohms.
16	INPUT connectors	Provide a means to connect the speaker and the meter to an external source. The voltage applied to the red connector should be positive with respect to the voltage at the black connector when the POLARITY switch is in the NOR position.
17	POLARITY switch	Provides a means to reverse the polarity of the dc meter.
18	TP2 TRIGGER switch	Selects TP2 triggering mode.
19	FUNCTION switch	Switches the meter circuit for the desired meter use.
20	COUNTS test point	Delivers a signal consisting of a pulse for every 100 errors recorded on the internal counter.
21	RANGE switch	Switches the meter to the desired operating range. Adjusts speaker volume when the FUNCTION switch is in the SPKR position.
22	CLOCK test point	Delivers a signal consisting of a 4.5-volt square wave with the same frequency as the test set bit rate.
23	TP1 TRIGGER switch	When lighted, indicates preselected signal appeared first on TP1 lead.
24	FIRST TP1 lamp	Selects TP1 triggering mode.

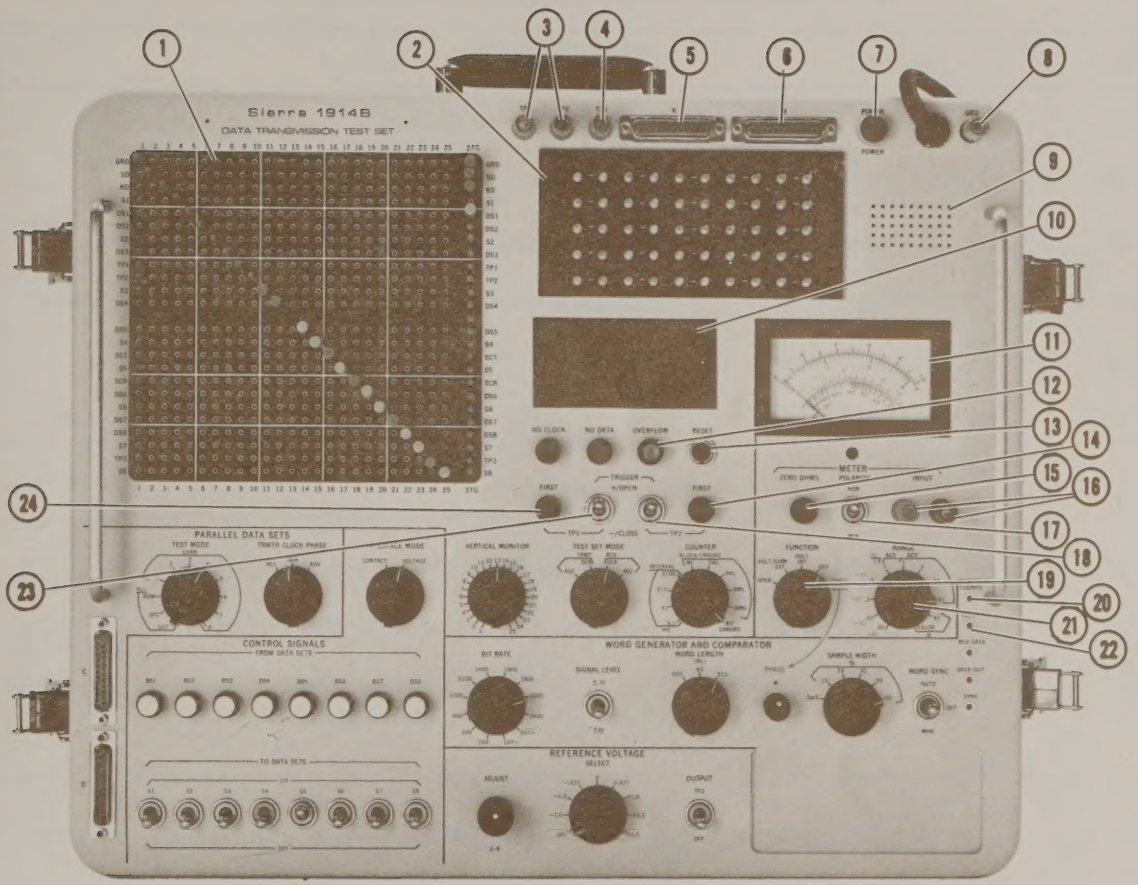


Figure 4. Sierra 1914B Data Transmission Test Set, Front Panel

Table 1. Front-Panel Controls, Indicators, and Connectors (Cont)

KEY	DEVICE	FUNCTION
25	RCV DATA test point	Delivers the data signal from the RD horizontal bus of the matrix, when the test set is in the serial receive mode.
26	DATA OUT test point	Delivers the bipolar data signal produced by the word generator.
27	SYNC test point	Delivers the positive word sync signal.

Table 1. Front-Panel Controls, Indicators, and Connectors (Cont)

KEY	DEVICE	FUNCTION
28	WORD SYNC switch	Selects either manual or automatic word synchronization.
29	SAMPLE WIDTH switch	Selects width of sample pulse.
30	PHASE adjustment	Used for fine adjustment of the bit synchronization circuits.
31	COUNTER switch	Permits measurement of block error rate, bit error rate, or interval.
32	WORD LENGTH switch	Selects dot, 63-bit, or 511-bit test word.
33	OUTPUT switch	When in the TP3 position, delivers the selected reference voltage to test point TP3 and to the TP3 horizontal bus of the matrix.
34	TEST SET MODE switch	Provides the appropriate test mode for the data set under test.
35	SELECT switch	Enables selection of a reference voltage.
36	SIGNAL LEVEL switch	Selects either ±0.7 or ±4 volts for SD output level.
37	ADJUST control	Used for coarse and fine adjustment of the reference voltage when the SELECT switch is in the ADJ position.
38	BIT RATE switch	Sets rate of timing signal used to drive word generator and comparator.
39	VERTICAL MONITOR switch	Provides a means of connecting the dc voltmeter to any of the interface leads of the data set.
40	INTERFACE MODE switch	Selects contact or voltage mode for control signals.
41	TRMTR CLOCK PHASE switch	Sets phase relationship of clock and parallel data signals.
42	S1–S8 switches	Apply control signals to the correspondingly numbered horizontal buses on the matrix.
43	DS1 to DS8 lamps	When lighted, indicate presence of control signals on the correspondingly numbered horizontal buses of the matrix.
44	Connector D	Provides connection to receiving 402-type data sets.
45	Connector C	Provides connection to transmitting 402-type data sets.
46	TEST MODE switch	Provides a means of applying the desired test signal to the parallel data channels.
47	NO CLOCK lamp	When lighted, indicates absence of clock signals.
48	NO DATA lamp	When lighted, indicates absence of data signal.

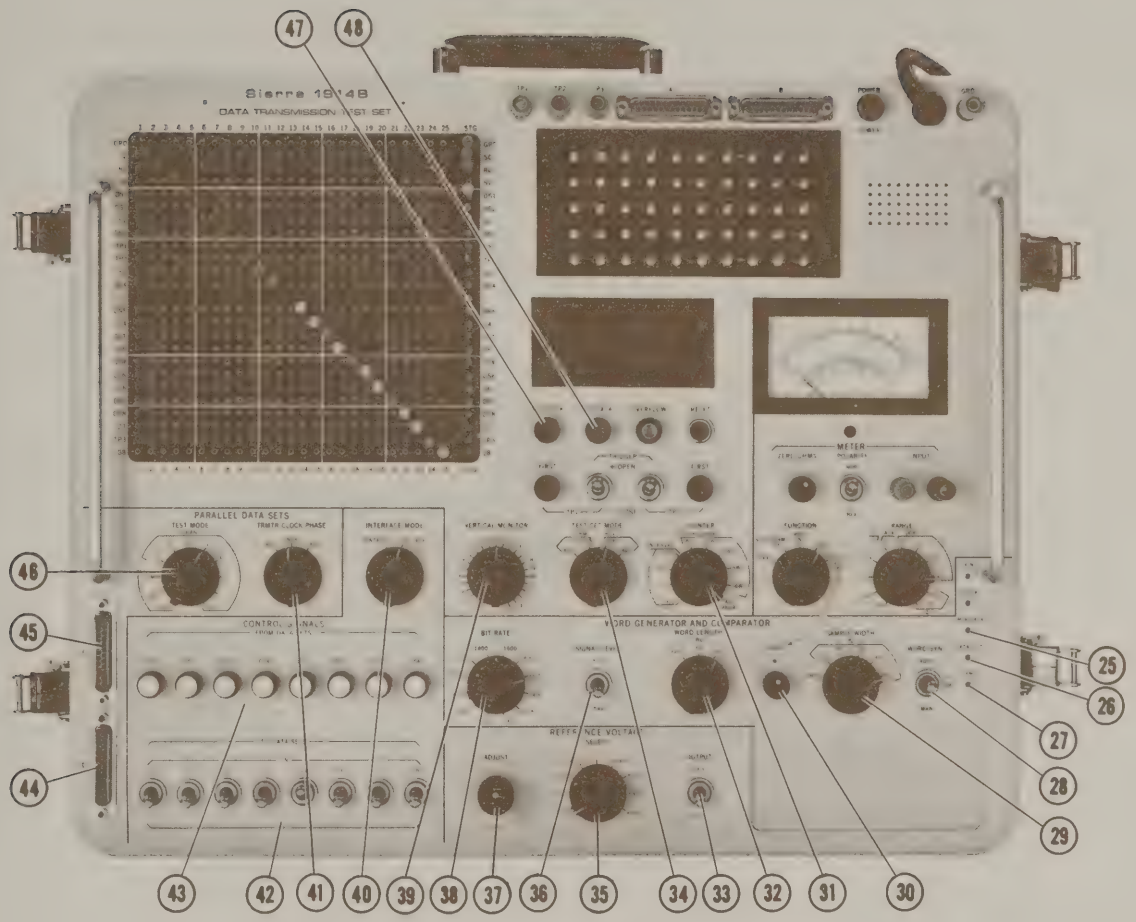


Figure 5. Sierra 1914B Data Transmission Test Set, Front Panel

3. FUNCTIONAL DESCRIPTION

3.01 The functional description of the 1914B is presented in four parts – overall function, serial transmit and receive functions, parallel data transmit function, and parallel data receive function.

Overall Function (Figure 6)

3.02 The program matrix provides the means for connecting the data set interface leads to the 1914B test circuits in the desired manner. The matrix consists of 24 horizontal and 25 vertical buses. The vertical buses connect through selector switches and connector A or B to the interface leads of the data set being tested. The horizontal buses connect to the various 1914B test circuits. Connection between a vertical bus and a horizontal bus is made by a pin inserted in the matrix. When series resistance is to be inserted at the connection, special pins with built-in resistors are used. Each of the 25 interface leads is shunted by a 300-kilohm resistor to provide marginal open-circuit loading for contact interfaces. Table 2 describes the test signals available at each of the horizontal buses of the matrix.

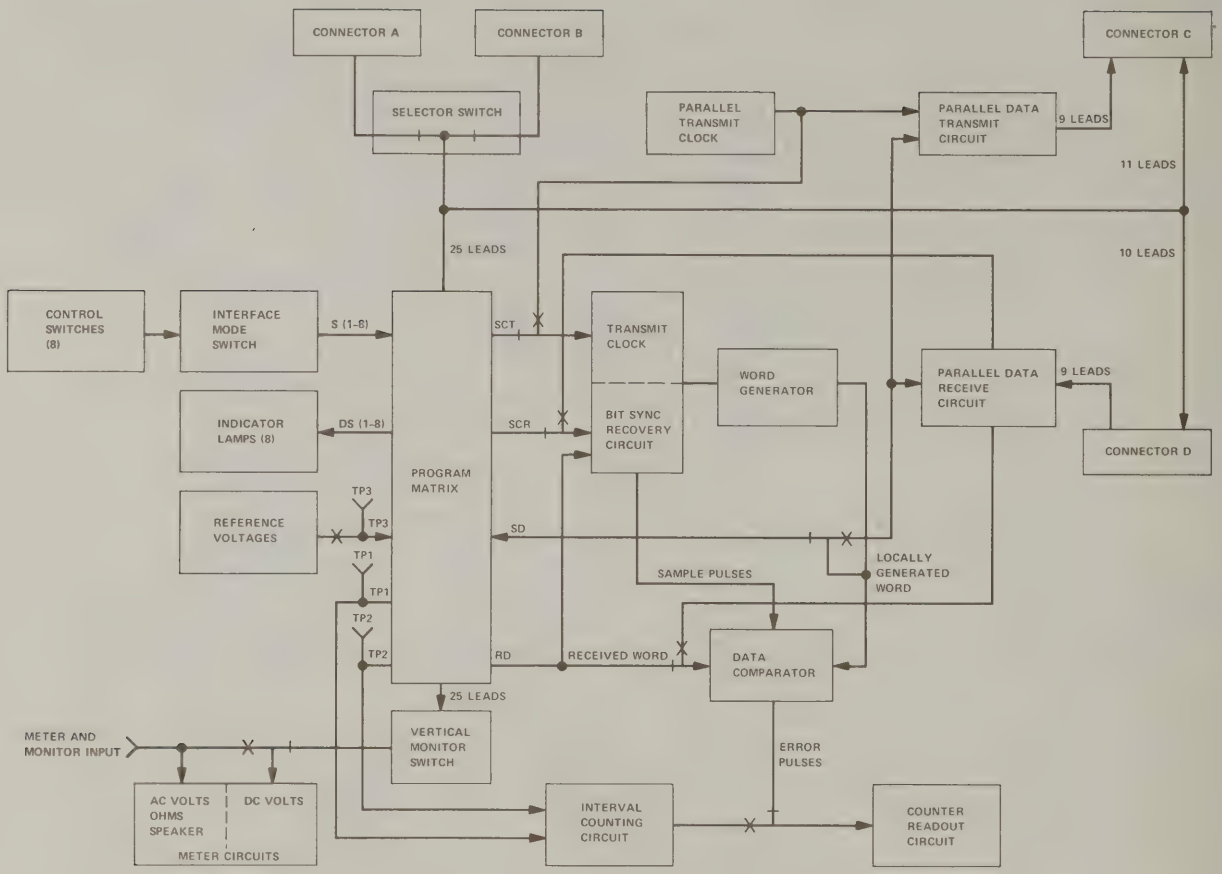


Figure 6. Overall Functional Block Diagram

Table 2. Signals Available on Program Matrix Horizontal Buses

HORIZONTAL BUS	SIGNAL
GRD	Test set ground.
SD	Send Data signals when the TEST SET MODE switch is in the TRMT position.
RD	Receive Data signals when the TEST SET MODE switch is in the RCV position
S1–S8	Control signal from the test set, present when the corresponding front-panel switch S1–S8 is in the ON position. The signal is either a ±4-voltage level or a contact closure, depending on the position of the INTERFACE MODE switch.
DS1–DS8	Control signal from the data set. When present corresponding front-panel lamp DS1–DS8 is lit. With the INTERFACE MODE switch in the CONTACT position, a contact closure to ground on a horizontal bus lights the corresponding indicator lamp. When the INTERFACE MODE switch is in the VOLTAGE position, a +3-volt signal present on a horizontal bus activates the lamp driver, which in turn lights the corresponding lamp.

Table 2. Signals Available on Program Matrix Horizontal Buses (Cont)

HORIZONTAL BUS	SIGNAL
TP1, TP2	Inputs to the test set interval counting circuit. These buses are also connected to front-panel test jacks TP1 and TP2, respectively, and may be used for connecting external signals to these matrix buses when the COUNTER switch is in any of the ERRORS positions.
SCT	Transmit clock signal.
SCR	Receive clock signal.
TP3	The signal applied to front-panel test jack TP3 when the OUTPUT switch is in the OFF position; or, when the OUTPUT switch is in the TP3 position, the reference voltage selected by the SELECT switch.

3.03 Each of the 25 interface selector switches has an A section and a B section, corresponding to interface connectors A and B. The switches are normally closed, and must be opened for additional functions. When both sections of a switch are closed, the corresponding pins of connectors A and B are interconnected. The latter mode of operation is useful when, for example, a business machine is connected to connector B and the data set is connected to connector A to provide a setup for in-service testing. By closing both the A and B sections of an interface selector switch, the signal on that particular lead becomes available on a vertical bus of the program matrix in a bridging connection. Any lead between the terminal and the data set can also be opened for testing the signals at either the terminal or data set by opening or closing the A or B section of the appropriate interface selector switch.

3.04 The meter circuits permit the operator to measure dc voltage, ac voltage, resistance, and signal level in dBm (600-ohm line calibration). When ac volts or ohms are to be measured, the circuit to be measured must be connected to the METER INPUT terminals. An audio signal on a line connected to the METER INPUT terminals can be monitored on the built-in loudspeaker by turning the FUNCTION switch to the SPKR position.

3.05 The VERTICAL MONITOR switch can be used to select a vertical matrix bus whose dc voltage is to be measured, or the dc voltage to be measured can be applied to the METER INPUT terminals.

3.06 The interval counting circuit measures the time interval between a signal on the TP1 bus and another signal on the TP2 bus (or test jacks TP1, TP2), and drives the front-panel digital display to indicate the interval in milliseconds or multiples thereof. The signal can be a positive or negative transition or a contact opening or closing, depending on the position of the TRIGGER switches. The signals can be applied to the counting circuit either from the matrix or from the front-panel TP1 and TP2 jacks. The interval counting circuit also determines which signal arrives first and indicates this information by means of the TP1 FIRST or TP2 FIRST lamp.

3.07 The reference voltage circuit provides fixed voltages of ±0.477, ±1, ±2, and +7 volts, and an adjustable voltage of 0 to 8 volts. The desired voltage is selected by the REFERENCE VOLTAGE SELECT switch and is delivered to the front-panel TP3 jack and the TP3 matrix bus when the OUTPUT switch is in the TP3 position.

3.08 A power supply in the 1914B provides two unregulated outputs of +23 and +200 volts and three regulated outputs of +12, -12, and +5 volts for operation of all of the test set circuits. Input to the power supply is 105 to 125 V, 48 to 65 Hz.

Serial Transmit and Receive Function (Figure 7)

3.09 The same clock circuit is used in both the transmit and receive modes. The clock rate is set by the front-panel BIT RATE switch. When this switch is in either of the EXT positions, the timing signal present on the SCT or SCR bus will drive the test set. In testing receiving asynchronous data sets, the clock circuits recover the bit timing signal from the incoming received data stream. The bit synchronization recovery circuit, therefore, controls the clock rate in the receive mode; the PHASE control permits precise synchronization with the incoming data signal.

3.10 The clock signal, either internal or external is applied to the word generator, which generates a dot signal (alternate marks and spaces), 63-bit test words, or 511-bit test words, depending on the setting of the WORD LENGTH switch.

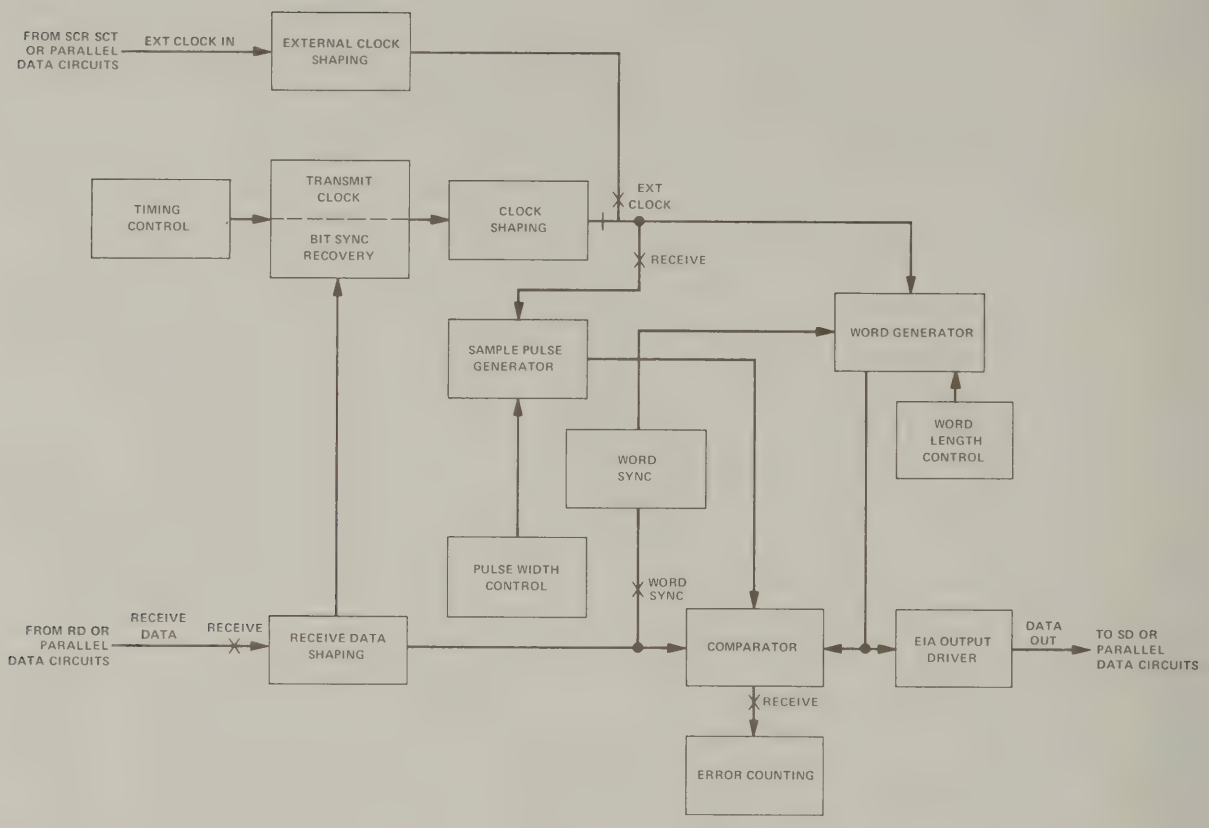


Figure 7. Serial Transmit and Receive Circuits

3.11 Errors in the received data signal are detected by comparing it with a test signal that is identical to the transmitted test signal. The comparison requires that the received and the locally generated test signals be synchronized, i.e., that the corresponding bits of the two test signals be aligned. Word synchronization is accomplished either manually or automatically, depending on the setting or the WORD SYNC switch.

3.12 When the WORD SYNC switch is momentarily depressed to the MAN position, the receiving test signal generator is forced into synchronism with the received test signal within a small fraction of a second. When the WORD SYNC switch is set to the AUTO position, the receiving test signal generator is continuously resynchronized with the received test signal. Because of the method of synchronization, the error count recorded in the AUTO mode is approximately three times the true error count.

3.13 The received data signal is compared with the locally generated test signal only during a short sampling interval coincident with the center of each received bit. In tests of asynchronous data sets, the sampling interval can be lengthened to include greater portions of the bit. Any discrepancy between the received bit and the locally generated bit during the sampling interval is registered as an error. The SAMPLE WIDTH switch selects the width of the sample interval in steps of 10 percent of the bit interval up to a maximum of 50 percent. This variable-width sampling technique allows checking the error margin of the received signal.

3.14 With the COUNTER switch set to the BIT ERRORS position individual bits in error are counted. When the COUNTER switch is set to one of the BLOCK ERRORS positions, the number of blocks of the selected length that contain one or more errors is counted. The block length is selected as the indicated multiple (i.e., WL, 2WL, etc.) of the word length (i.e., 63 or 511). The minimum block length is 63 bits, the maximum is in excess of 8000 (16 x 511) bits.

Parallel Data Transmit Circuits (Figure 8)

3.15 The dot generator, driven by the 75-Hz parallel transmit clock multivibrator, produces a 75-bps dotting signal. In the ALL DOT position of the TEST MODE switch, this signal is applied through output drivers and connector C to the eight parallel data channels. The output drivers provide the contact closure type of interface required by parallel data sets. The control leads of the data set appear on the matrix.

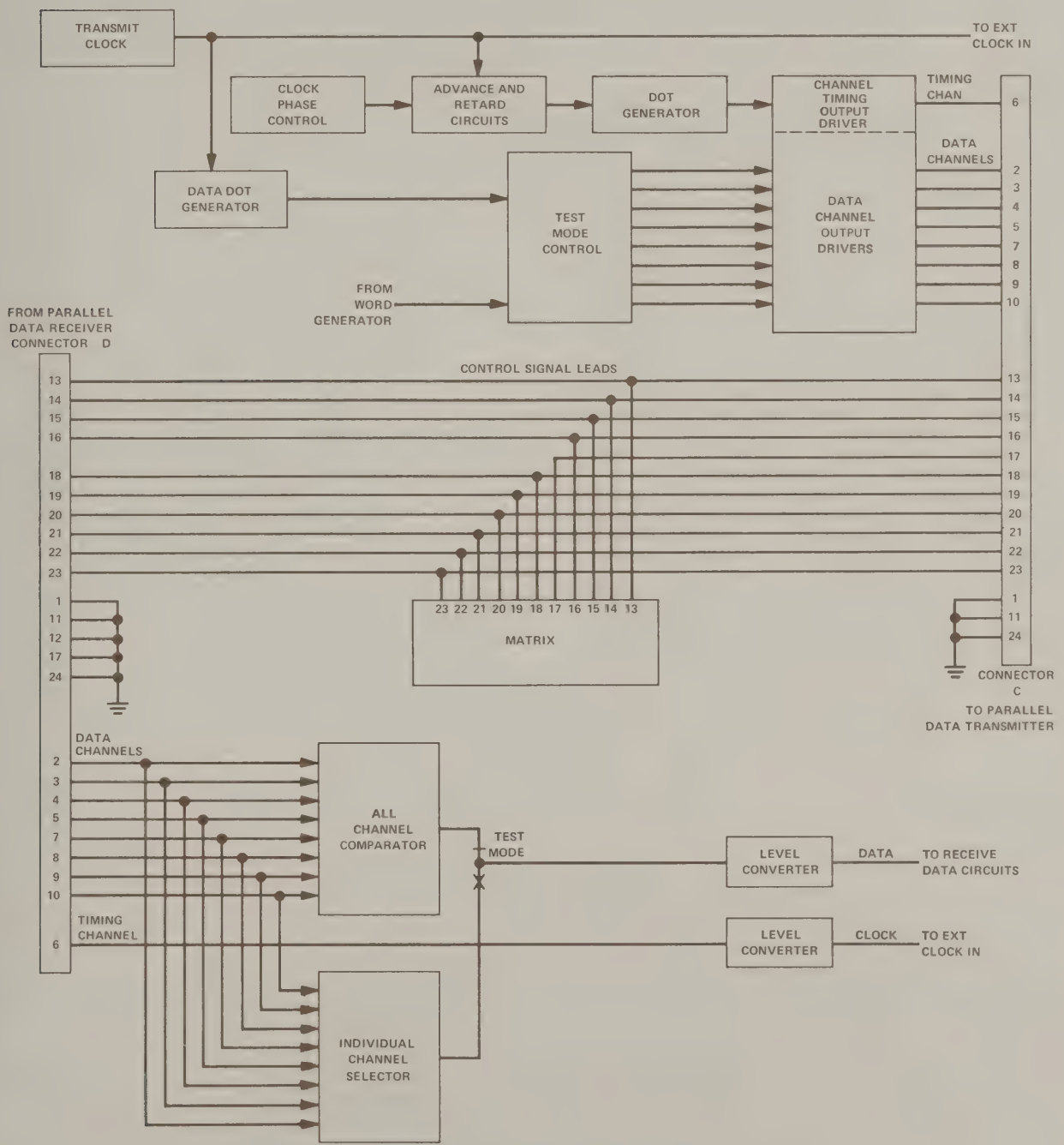


Figure 8. Parallel Transmit and Receive Circuits

3.16 In the ALL RDM position of the TEST MODE switch, test words from the word generator are applied to all eight parallel data channels. In the ALL SPC position of the TEST MODE switch, a space signal is applied to the eight channels, while in any one of the CHAN positions of the switch, test words are applied to the selected channel and the dot signal is applied to the other channels.

3.17 The output of the dot generator is also applied to the timing channel of the parallel data set. By means of the TRMT CLOCK PHASE switch, this dot signal can be advanced or retarded in phase by 1.5 milliseconds with respect to the data signal to simulate changes in phase relationship between the clock and data signals.

Parallel Data Receive Circuits (Figure 8)

3.18 Connections from the receiving parallel data set to the test set are made through connector D, the control leads again are connected to the matrix. If the data channels are to be tested individually, the TEST MODE switch is turned to the desired channel, and error checks are made in the same way as for serial data sets, as described in paragraphs 3.09 through 3.14.

3.19 If all channels are to be tested simultaneously, the TEST MODE switch is turned to ALL RDM. The combined output from all channels is compared to the output of the word generator. If any channels contain errors, the errors will be registered on the counter display.

3.20 The signal on the timing channel is applied through the level converter to the external clock input of the word generator and drives the word generator and comparator circuits.

4. SPECIFICATIONS

4.01 The signal outputs of the 1914B are accessible at the program matrix and the various test points on the front panel. Table 3 lists the specifications.

5. OPERATION

5.01 This section of the manual explains the operation of the matrix, the selector switches, the interval counter, the meter, and the loudspeaker, and it describes typical tests of serial data sets and analog data sets. For detailed operating instructions for a particular type of data set and for detailed test requirements, refer to local procedures or to the modem manufacturer's recommendations.

Table 3. Specifications

Parameter	Characteristic
SD (Send Data)	Bipolar, NRZ (nonreturn to zero) signal, ±3.5 to ±5 volts or ±0.7 volt in amplitude from an impedance of 200 ohms with rise and fall times not exceeding 1 μsec.
S1-S8 Control Signals	±3.5 to ±5 volt dc levels in the voltage mode, contact closures to ground and open circuits in the contact mode.
Internal Clock Bit Rates	150, 300, 600, 1000, 1200, 1400, 1600, 1800, 2000, and 2400 bits per second ±3%.
RD (Receive Data)	Bipolar, NRZ (nonreturn to zero) signal, minimum amplitude ±3 volts; input resistance 2400 ohms in series with a silicon diode junction.
SCR (Serial Clock; Receive)	Bipolar square wave, minimum amplitude ±3 volts; input resistance 2400 ohms in series with a silicon diode junction.
SCT (Serial Clock; Transmit)	Same as SCR.
DS1-DS8 Voltage Mode	+3 dc level to light lamp; input resistance 3000 ohms in series with a silicon diode junction.
DS1-DS8 Contact Mode	Contact closure to ground to light lamp; lamp current 40 mA, lamp voltage +23 volts.

Table 3. Specifications (Cont)

PARAMETER	CHARACTERISTIC
Received Bit Rates (Internal Clock)	150, 300, 600, 1000, 1200, 1400, 1600, 1800, 2000, and 2400 bits per second ±5%.
Power Required	105–125 Vac, 48–65 Hz, approximately 60 watts.
Operating Temperature Range	+40° to +120°F
Dimensions	Width 18-1/2 inches, Height 15 inches, Depth 7-1/2 inches.
Weight	27 pounds (approximate).

5.02 Carefully unpack and inspect each instrument for damage. If any evidence of damage is observed, contact:

Customer Service Department
Sierra Electronic Operation
Philco-Ford Corporation
3885 Bohannon Drive
Menlo Park, California 94025
Telephone (415) 322-7222

NOTE: Do not repackage damaged or faulty equipment for return to Sierra Electronic Operation under the provisions of the warranty without first contacting Sierra for specific instructions.

5.03 **Program Matrix:** The matrix, which provides a convenient means of interconnecting the data set interface leads with the test set circuits, is described in detail in Paragraph 3.02. Red pins provide a direct connection between the horizontal and vertical buses; gray pins and green pins make the interconnections through built-in 10-ohm and 18-ohm resistances, respectively. The resistors simulate cable resistance.

5.04 **Interface Selector Switches:** Figure 9 is a schematic diagram of the interface selector switches. The switches consist of an A and a B section, each of which is a combination switch and test point. This feature makes all interface signals accessible for external connections and also permits testing modems with the terminal equipment connected to the test set. By selectively closing and opening

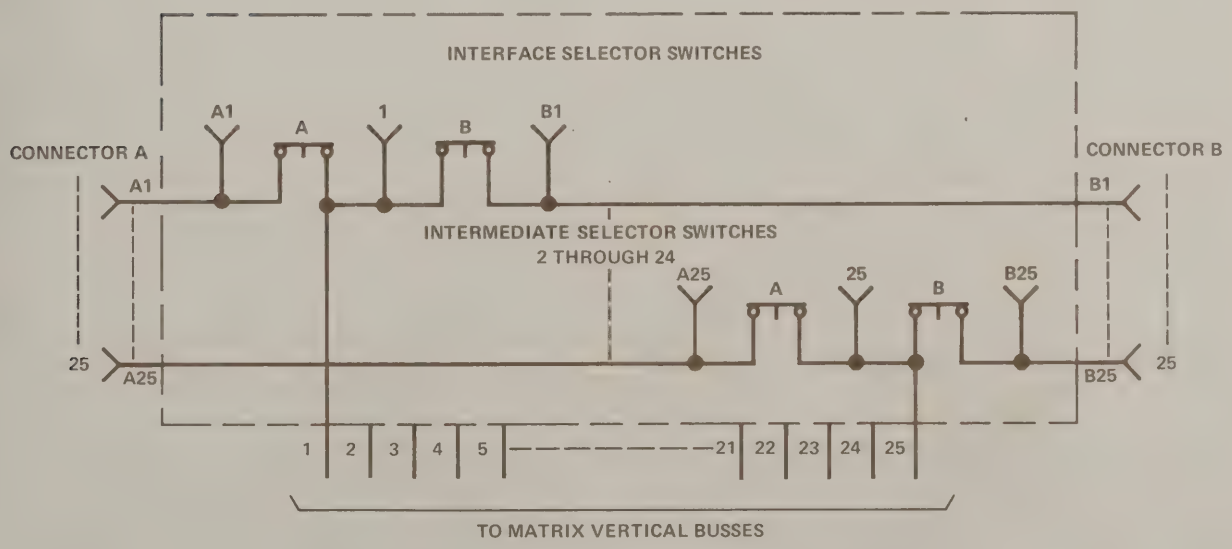


Figure 9. Interface Selector Switches, Schematic Diagram

individual interface leads, signal flow between the modem and the terminal equipment can be checked by the test set in a bridging or terminating mode.

5.05 **Interval Counter:** The interval counter can be used to check the sequence in which control leads are actuated and the time delays involved can be measured. The counter is described in detail in Paragraph 3.06, and its use is described below.

5.06 To measure the interval between two signals, proceed as follows:

Step 1
Apply the signals to be measured either directly to TP1 and TP2, or to the TP1 and TP2 horizontal matrix buses by means of shorting pins.

Step 2
Set the TRIGGER TP1 switch depending on the expected TP1 signal and set the TRIGGER TP2 switch in accordance with anticipated signal on TP2.

Step 3
Set the COUNTER switch to the appropriate range for the interval to be measured.

Step 4
Set the BIT RATE switch to any internal bit rate.

Step 5
Set the TEST SET MODE switch to TRMT SER.

Step 6
Press the RESET switch momentarily to clear the counter.

Step 7
When the measurement takes place, the number in the counter display multiplied by the factor selected by the COUNTER switch will be the measured interval in milliseconds.

Step 8
If the FIRST TP1 lamp lights, it means that the signal on TP1 occurred before the signal on TP2; conversely, if the FIRST TP2 lamp lights, it means that the signal on TP2 occurred before the signal on TP1.

5.07 In addition to measuring the interval between two signals, pulse duration can be measured by applying the same signal to both the TP1 and TP2 leads. To measure, for example, a positive pulse, set the TRIGGER TP1 switch to +/OPEN and the TRIGGER TP2 switch to -/CLOSE. The interval so measured is the pulse width.

5.08 **Meter:** The front-panel meter can be used for the following purposes:

(a) To measure dc voltages on the interface leads.

(b) To measure ac voltages, dc voltages, or resistance to ground of an external circuit.

NOTE: One side of the ohmmeter is grounded.

5.09 To measure dc voltages on the interface leads, place the FUNCTION switch in the VOLT INT position, turn the RANGE switch to the appropriate dc range, and turn the VERTICAL MONITOR switch to the desired interface lead number. The NOR position of the POLARITY switch gives an up-scale reading for positive inputs.

5.10 To measure ac voltage, dc voltage, or resistance to ground in an external circuit, connect the circuit to the INPUT terminals, turn the FUNCTION switch to VOLT/OHM EXT, and turn the RANGE switch to the appropriate voltage or resistance range. The ac meter input is a balanced high-impedance circuit to produce minimum loading when connected across a telephone line.

CAUTION: Damage may result to the meter when measuring line signals (FUNCTION switch set to EXT) if the RANGE switch is inadvertently placed in the DCV or X1, X100 (ohms) position. The FUNCTION switch should be set to OFF when the set is being transported.

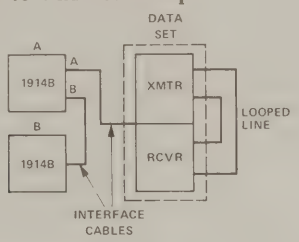
5.11 **Loudspeaker:** To audibly monitor the signal on a line, connect the line to the INPUT terminals, turn the FUNCTION switch to SPKR, and adjust the volume with the RANGE switch in its ACV positions. The ability to listen to the line signals is, at times, helpful in identifying system problems. Noise, clicks, and crosstalk, for example, can frequently cause data transmission problems.

Testing Serial Data Sets

5.12 Connect the data set to the test set by means of the A or B connector. Insert pins in the program matrix for the proper interconnections between the data set and the test set. Set the INTERFACE MODE switch to VOLTAGE or CONTACT as required; this setting will usually be VOLTAGE for serial data sets. Set switches S1 through S8 to place control signals on the appropriate interface leads, and observe lamps DS1 through DS8 for the proper response.

5.13 The most common test is the end-to-end test which is depicted in Figure 10a. The overall performance of the total system, i.e., transmitting data set, telephone line, receiving data set, is checked in this test. The test set at the transmitter and receiver location are operated in the transmit and receive modes, respectively. Upon completion of the tests in the direction shown – if the system being tested is half-duplex or full duplex, the tests can be repeated in the opposite direction.

A. Typical End-to-End Test Setup



B. Typical Loop-around Test Setup

Figure 10. Typical Test Setups

5.14 To test a full-duplex data set back-to-back, the line signal output from the transmitter must be looped back to the receiver line input. The test still requires two 1914B test sets, one operating as a controlling test set (A) and the second as a slave unit as shown in Figure 10b. Set A is connected to the data set by means of the interface cable which carries both the transmit as well as the receive signals. Set A should be programmed to operate all the control functions of the data set; test set B functions only as a data generator or comparator. The connections between sets A and B are most easily established by means of a second interface cable. Set B is programmed to connect to only the transmit (i.e., SD, SCT) or receive (i.e., RD, SCR) signal leads. The actual test is performed in the normal manner as described in 5.16 through 5.19.

5.15 The input/output leads of the test set are assigned to the horizontal buses of the matrix in such an order that the program for most data sets requires placing pins approximately along a diagonal line, as shown in Figure 11 which is intended as an illustration only. Pin 1 of the interface (EIA circuit AA; CCITT-circuit 101) is connected to the GRD bus as is pin 7 (circuit AB; 102). Pin 2 (BA; 103) connects to the SD bus which carries the word generator output. Similarly, pin 3 (BB; 104) is connected to the RD bus, which accepts the received data input when the test set is in the receive mode. The transmit and receive clock signals from the data set (circuits DB, DD; 113, 115), respectively, appear on the SCT and SCR buses. Switches S1, S5, S6, and S7 apply control signals to the "Send Request" lead (CA; 105), the "Data Terminal Ready" lead (CD; 108), the "Secondary Request to Send" lead (SCA; 120), and to the "Data Signal Rate Selector" lead (CH/CI; 111/112), respectively. S4 is used to simulate a low-speed "Secondary Transmitted Data" input (lead SBA; 118). Lamps DS1 through DS8 are programmed to monitor the output of the data set on, respectively, the "Clear to Send" lead (CB; 106), the "Data Set Ready" lead (CC; 107), the "Received Line Signal Detector" lead (CF; 109), the "Secondary Line Signal Detector" lead (SCF; 122), the "Secondary Clear to Send" lead (SCB; 121), the low-speed "Secondary Received Data" Signal lead (SBB; 119), the "Signal Quality Detector" lead (CG; 110), and the "Ring Indicator" lead (CE; 125).

5.16 **Indicator Lights:** If the NO DATA or NO CLOCK lamp lights during an error rate test, a malfunction is indicated. The malfunction must be present for several seconds to light these lamps.

5.17 **Transmitting Tests – Synchronous or Asynchronous Data Sets:**

Step 1
Set the TEST SET MODE switch to TRMT SER.

Step 2
For synchronous data sets, set the BIT RATE switch to EXT + or EXT –, depending on the desired phase relationship of clock signal to data signal; this setting will usually be EXT +.

For asynchronous data sets, set this switch to the appropriate bit rate.

Step 3
Set the SIGNAL LEVEL switch to the required position, for data sets conforming to EIA or CCITT specifications the signal level must be ±4 volts.

Step 4
Set the WORD LENGTH switch for the desired test signal.

5.18 **Receiving Tests – Synchronous Data Sets:**

Step 1
Set the TEST SET MODE switch to RCV SER.

Step 2
Set the WORD LENGTH switch to agree with the transmitted word.

Step 3
Set the COUNTER switch to BIT ERRORS or BLOCK

ERRORS, as required. Block errors can only be counted with the WORD LENGTH switch set to 63 or 511.

Step 4

Set the BIT RATE TO EXT + or EXT – depending on the desired phase relationship of clock signal to data signal (normally EXT +).

Step 5

Operate the WORD SYNC switch momentarily to MAN or set the switch to AUTO.

Step 6

Press the RESET switch momentarily to clear the counter.

Step 7

Observe the recorded error count on the counter display.

NOTE: With the WORD SYNC switch set to the AUTO position, the error count displayed equals very nearly three times the true number of errors.

5.19 Receiving Tests – Asynchronous Data Sets:

Step 1
Set the TEST SET MODE switch to RCV SER.

Step 2
Set the WORD LENGTH switch to agree with the transmitted word.

Step 3
Set the COUNTER switch to BIT ERRORS or BLOCK ERRORS as required. Block errors can only be counted when the WORD LENGTH switch is set to 63 or 511.

Step 4
Set the PHASE control to mid position, with the dot pointing up.

Step 5
Set the BIT RATE switch to agree with the transmitted bit rate

Step 6
Set the FUNCTION switch to PHASE ADJ.

Step 7
Adjust the PHASE control for a null on the meter.

Step 8
Set the FUNCTION switch to some position other than PHASE ADJ (do not return to PHASE ADJ during remainder of test).

Step 9
Set the SAMPLE WIDTH switch to .5 μs.

Step 10
Operate the WORD SYNC switch momentarily to MAN, or set it to AUTO.

Step 11
Set the SAMPLE WIDTH switch to the desired sampling interval for error margin testing.

Step 12
Press the RESET switch momentarily and observe the recorded error count on the counter display.

NOTE: With the WORD SYNC switch set to the AUTO position, the error count displayed equals very nearly three times the true number of errors.

Testing Parallel Data Sets

5.20 The tests described in the following paragraphs were designed for the WECO 402 type of modems.

5.21 Connect the data set to the C (transmit) or D (receive) connector. Insert pins in the program matrix for the proper interconnections of the interface control leads between the data set and the test set. (Refer to Figure 7.) Set the INTERFACE MODE switch to the CONTACT position. Set switches S1 through S8 to place control signals on the appropriate interface leads and observe lamps DS1 through DS8 for the proper response. Set the TEST MODE switch to ALL SPC to place a spacing condition on all channels, to ALL DOT to apply alternate marks and spaces to all channels, or to one of the eight channels to place a test word on that channel while applying a dot signal to all other channels.

NOTE: If the NO DATA or NO CLOCK lamp lights during an error rate test, a malfunction is indicated.

5.22 Transmitting Tests:

Step 1
Set the WORD LENGTH switch to select the desired test signal.

Step 2
Set the SIGNAL LEVEL switch to ±4 volts.

Step 3
Set the BIT RATE switch to EXT +.

Step 4
Set the TEST SET MODE switch to TRMT 402.

Step 5
Set the TEST MODE switch to ALL RDM to test all eight channels simultaneously or any one channel individually.

Step 6

Set the TRMT CLOCK PHASE switch to RET, NOR, or ADV, as required. In an end-to-end test this control at the transmitting data test set may be set to the ADV or RET position which will change the phase relationship between the clock signal and the data signal by 1.5 ms. This establishes a marginal condition which will normally result in increased errors at the receiving data set.

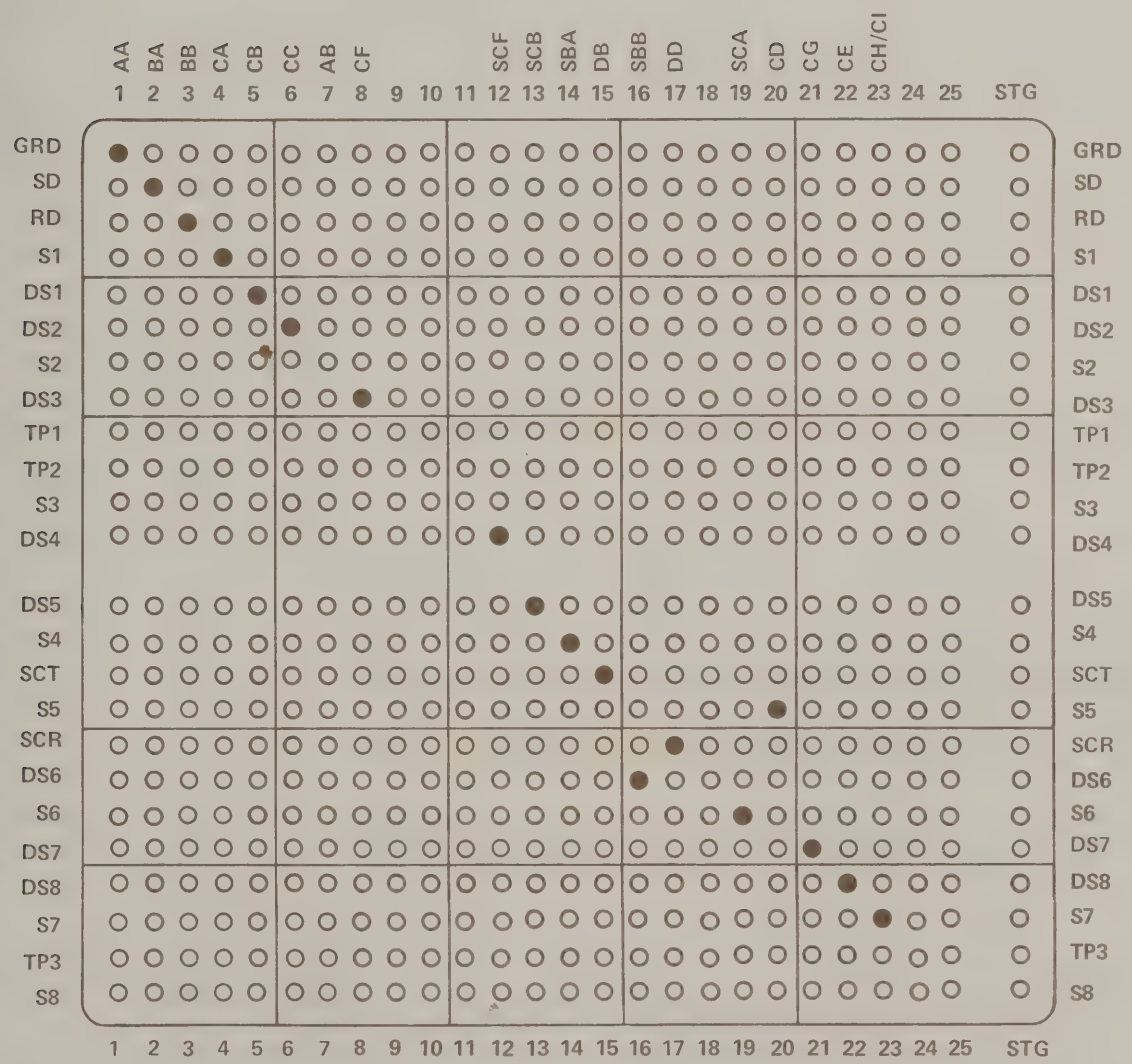


Figure 11. Sample Program of Matrix

5.23 **Receiving Tests:**

Step 1
Set the TEST SET MODE switch to RCV 402.

Step 2
Set the COUNTER switch to BIT ERRORS or BLOCK ERRORES as required.

Step 3
Set the TEST MODE switch to ALL RDM to test all eight channels simultaneously; set the switch to CHAN/1-8 to check any channel individually

Step 4
Operate the WORD SYNC switch momentarily to MAN or set it to AUTO.

Step 5
Press the RESET switch momentarily to clear the counter.

Step 6
Observe the recorded error count on the counter display.

NOTE: With the WORD SYNC switch set to the AUTO position, the error count displayed equals very nearly three times the true number of errors.

Testing Analog Data Sets

5.24 Analog data sets can be tested by applying precision dc voltages to the transmitter (SD lead) and measuring the receiver (RD) output voltage. The interface connections are established on the program matrix and the data set control functions are checked by using S1 through S8 and DS1 through DS8, as discussed in 5.12 – 5.15.

5.25 **Transmitting Tests:**

Step 1
Set the REFERENCE VOLTAGE SELECT switch to the desired fixed voltage or to the ADJ position.

Step 2
Set the OUTPUT switch to TP3.

Step 3
Insert a shorting pin at the intersection of the TP3 horizontal bus and the vertical bus connected to the SD lead.

Step 4
Set the VERTICAL MONITOR switch to the position corresponding to the SD interface lead.

Step 5
If the adjustable voltage is to be used, turn the FUNCTION switch to VOLT INT, and the RANGE switch to the appropriate DCV range. Using the meter, set the voltage to the desired value.

5.26 **Receiving Tests:**

Step 1
Set the VERTICAL MONITOR switch to the position corresponding to the RD interface lead.

Step 2
The measured voltage should be the same, both in magnitude and polarity, as the transmitted voltage within the modem manufacture's specified circuits.

5.27 **4-dB Pad.** The 4-dB pad may be shunted across the output line of the transmitting data set during error rate tests. The resultant bridging loss reduces the signal level by about 4 dB and, therefore, also reduces the signal-to-noise ratio at the receiving data set. Consequently, the test conditions are more stringent than those encountered during normal operation of the data set.

6. MAINTENANCE

6.01 Section 6 gives information to enable the operator to check a 1914B test set to see if it is operating within specifications. The tests will enable the operator to isolate a trouble to a lamp, fuse, or replaceable circuit pack. Most of the tests can be performed without any external test equipment. However, the tests of Paragraphs 6.10, 6.11, and 6.12 require an electronic counter, a dual-trace oscilloscope, and a signal generator, respectively. More detailed test and troubleshooting information is contained in the Sierra Maintenance Manual, SMM-1914B, available upon request.

6.02 To gain access to the fuses, circuit packs, and the ac volt meter calibration control (R17), unplug the power cord and loosen the four quick-release fasteners at the rear of the 1914B. With the front panel facing up, lift the 1914B chassis out of its case. Figure 12 shows the location of the replaceable components.

6.03 The tests of Paragraphs 6.04 through 6.12 are performed on a single 1914B. Tests of Paragraphs 6.14 and 6.15 require an additional 1914B.

WARNING: Before proceeding with any test in this section, make sure that all test leads and matrix pins have been removed, all interface selector switches are depressed, and all interface connecting cables are free of shorts, opens, and crosses.

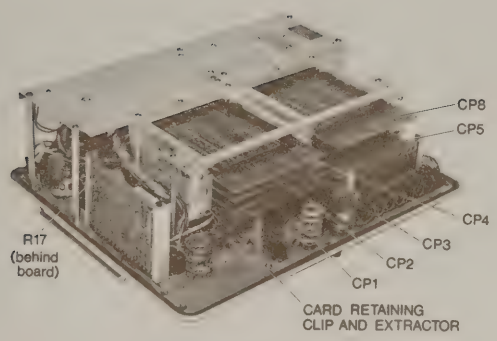


Figure 12. Location of Replaceable Components

If any fuses or lamps are to be replaced as the result of the tests, select replacements according to the following tabulation. Figure 13 shows the method of replacing lamps.

WARNING: Use only fuse types specified. Serious damage to the equipment may be caused by improper substitution.

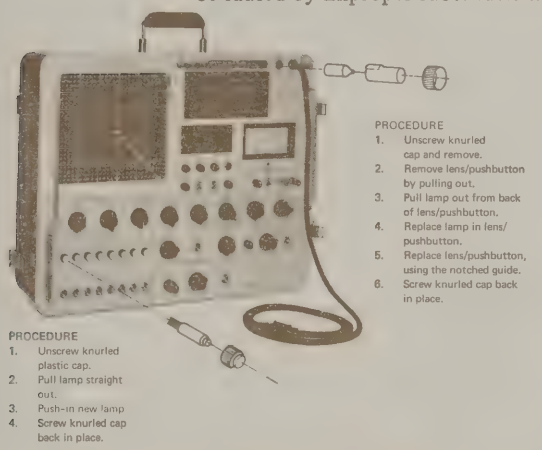

PROCEDURE
1. Unscrew knurled cap and remove.
2. Remove lens/pushbutton by pulling out.
3. Pull lamp out from back of lens/pushbutton.
4. Replace lamp in lens/pushbutton.
5. Replace lens/pushbutton, using the notched guide.
6. Screw knurled cap back in place.
PROCEDURE
1. Unscrew knurled plastic cap.
2. Pull lamp straight out.
3. Push-in new lamp
4. Screw knurled cap back in place.

Figure 13. Lamp Replacement Procedure

FUSES	REPLACEMENT PARTS
F1	1/2 amp Type MDL Bussman
F2	0.6 amp Type AGC Bussman
F3	1/2 amp Type AGC Bussman
F4	3/8 amp Type AGC Bussman
F5	3/4 amp Type AGC Bussman

LAMPS

Power switch	A1G
All others	B0934 Sylvania

LENS

White	B0146 Sylvania
Blue	B0143 Sylvania
Red	B0142 Sylvania
Amber	B0140 Sylvania

SHORTING PINS

Red	919900046 Sierra
Gray 10Ω	919900047 Sierra
Green 18Ω	919900048 Sierra

CIRCUIT BOARDS

CP1	D02647100 Sierra
CP2	D02648500 Sierra
CP3	D02648600 Sierra
CP4	D02648700 Sierra
CP5	D02648800 Sierra
CP8	D02648900 Sierra

Tests on a Single 1914B

6.04 **Fuses:** By following the procedure below, the operator can determine when a fuse has failed. If a fuse is to be replaced, refer to Paragraph 6.03 for access instructions. Figure 14 shows the location of fuses and spare fuses.

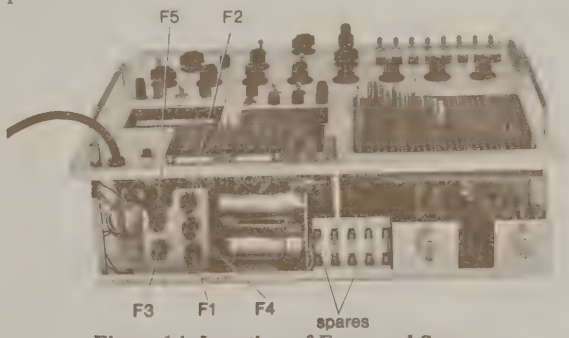


Figure 14. Location of Fuses and Spares

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Operate the POWER switch.	The POWER lamp lights and the set is operative.	Fuse F1
2	Set the TEST MODE switch to RCV SER, and set the BIT RATE switch to EXT +.	The NO DATA and NO CLOCK lamps light.	Fuse F2

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
3	Set the FUNCTION switch to VOLT INT and the RANGE switch to DC/10. Set the SELECT switch to +2.0 and the OUTPUT switch to TP3. Set the VERTICAL MONITOR switch to 1 and the POLARITY switch to NOR. At the matrix, insert a shorting pin in row TP3, column 1.	The meter reads 2.0 volts.	If the meter reads 0 in all the plus voltage positions of the SELECT switch, fuse F3 is probably defective.
4	Set the SELECT switch to -2.0 and POLARITY switch to REV. Remove the shorting pin in row TP3, column 1.	Meter reads 2.0 volts.	If the meter reads 0 in all of the minus voltage positions of the SELECT switch, fuse F4 is probably defective.
5	Set the FUNCTION switch to VOLT/OHM EXT. Set the one RANGE switch to X1. Short-circuit the INPUT terminals with a test lead. Adjust the ZERO OHMS control.	It should be possible to move the meter pointer to 0Ω (on ohmmeter scale) with the ZERO OHMs control.	Fuse F5

6.05 **Control Signals**: Either voltages or contact closures can be used as control signals with the 1914B test set. The following procedure checks the test set for operation with both types of control signals.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	At the matrix, insert a shorting pin in row S1, column 1; and insert a second shorting pin in row DS1, column 1. Set toggle switches S1 through S8 to OFF. Operate the POWER switch.	POWER lamp lights.	
2	Set INTERFACE MODE switch to CONTACT.	Lamps DS1 through DS8 are off.	
3	Set toggle switch S1 to ON.	Lamp DS1 lights.	Lamp DS1.
4	Settle toggle switch S1 to OFF.	Lamp DS1 goes off.	
5	Test the control circuits in accordance with Table A.	Lamps DS2 through DS8 operate as shown in Table A.	Lamps DS2 through DS8. . Circuit pack CP8. **NOTE**: If an indicator lamp fails to light with the INTERFACE MODE switch set to CONTACT, the corresponding position can be tested with

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
			the voltmeter. Set the FUNCTION switch to DCV/30, and select the desired matrix connection using the VERTICAL MONITOR switch. The meter will indicate 0 for a lamp failure. If the meter indicates +23 dc volts, the trouble is internal to the 1914B.
6	Set the INTERFACE MODE switch to VOLTAGE.	Lamps DS1 through DS8 remain off.	
7	Repeat Steps 3, 4, and 5.	Same as in Steps 3, 4, and 5 and Table A.	Lamps DS1 through DS8. Circuit pack CP8. **NOTE**: If an indicator lamp fails to light with the INTERFACE MODE switch set to VOLTAGE, the corresponding position can be tested with the voltmeter. Set the FUNCTION switch to VOLT INT, RANGE switch to DCV/10, and select the desired matrix connection using the VERTICAL MONITOR switch. A meter indication of +4.0 ±0.3 dc volts should be observed for toggle switches that are ON and –4.0 ±0.3 dc volts for switches that are OFF.
8	Operate the POWER switch.	POWER lamp goes off.	
9	Remove test connections.		

Table A. Operation of Control-Signal Lamps

MATRIX CONNECTIONS		TOGGLE-SWITCH SETTINGS		NORMAL INDICATIONS	
ROW	COLUMN	SWITCH	POSITION	LAMP	CONDITION
DS2	2	S2	ON	DS2	Lighted
S2	2		OFF		Off
DS3	3	S3	ON	DS3	Lighted
S3	3		OFF		Off

Table A. Operation of Control-Signal Lamps (Cont)

MATRIX CONNECTIONS		TOGGLE-SWITCH SETTINGS		NORMAL INDICATIONS	
ROW	COLUMN	SWITCH	POSITION	LAMP	CONDITION
DS4	4	S4	ON	DS4	Lighted
S4	4		OFF		Off
DS5	5	S5	ON	DS5	Lighted
S5	5		OFF		Off
DS6	6	S6	ON	DS6	Lighted
S6	6		OFF		Off
DS7	7	S7	ON	DS7	Lighted
S7	7		OFF		Off
DS8	8	S8	ON	DS8	Lighted
S8	8		OFF		Off

6.06 Interval Counter: The following procedure tests the interval counter's ability to detect the first occurrence of a preselected signal transition and also provides a test of the counter display.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITIONS
1	Set toggle switches S1 through S8 to OFF.		
2	Insert shorting pins in the following matrix positions: row TP1, column 1 row S1, column 1 row TP2, column 2 row S2, column 2.		
3	Turn FUNCTION switch to OFF.		
4	Operate POWER switch.	POWER lamp lights.	
5	Set INTERFACE MODE switch to CONTACT.		
6	Set BIT RATE switch to 2400.		
7	Set TEST MODE switch to TRMT SER.		
8	SET TRIGGER TP1 and TRIGGER TP2 switches to -/CLOSE.		
9	Set COUNTER switch to INTERVAL/X100.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
10	Momentarily operate the RESET switch.	Counter display reads 00.	
11	Using a suitable timer, set toggle switch S1 to ON.	Counter display starts.	
12	After 5 seconds, set toggle switch S2 to ON.	Counter display stopped at approximately 50. FIRST TP1 lamp lighted.	FIRST TP1 lamp.
13	Set TRIGGER TP1 and TRIGGER TP2 switches to +/OPEN.		
14	Momentarily operate the RESET switch.	Counter display reads 00.	
15	Using a suitable timer, set toggle switch S2 to OFF.	Counter display starts.	
16	After 5 seconds, set toggle switch S1 to OFF.	Counter display stopped at approximately 50. FIRST TP2 lamp lighted.	FIRST TP2 lamp.
17	Operate POWER switch.	POWER lamp goes off.	
18	Remove shorting pins from matrix.		

6.07 Word Generator and Clock: The following procedure tests the ability of the word generator to produce its three test messages – a dot signal, a 63-bit test message, and a 511-bit test message – and the ability of the clock to generate a timing signal over the range of 150 to 2400 bps.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect TP1 to the black INPUT connector and connect TP2 to the red INPUT connector.		
2	Set front-panel controls as follows: METER POLARITY SWITCH to REV. TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS. FUNCTION switch to OFF. BIT RATE switch to 1600.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
	SIGNAL LEVEL switch to ±.7V.		
	WORD LENGTH switch to 63.		
	WORD SYNC switch to OFF.		
3	Insert shorting pins in the following matrix positions: row GRD, column 1 row SD, column 2 row TP1, column 1 row TP2, column 2.		
4	Operate POWER switch	POWER lamp is lighted.	
5	Set RANGE switch to 1 VAC.		
6	Set FUNCTION switch to VOLT/OHM EXT.	NO DATA lamp is off.	CP1, CP2, CP4
		NO CLOCK lamp is off.	
		Meter indicates .60 ±0.05 Vac.	CP3, CP4
7	Set WORD LENGTH switch to 511.	Meter indicates .60 ±0.05 Vac.	CP3
8	Set WORD LENGTH switch to DOT.	Meter indicates .75 ±.075 Vac.	
9	Set FUNCTION switch to OFF.		
10	Set BIT RATE switch to 150.		
11	Set WORD LENGTH switch to 63.		
12	Set TEST SET MODE switch to RCV SER.	Counter display indicates counting.	
		NO DATA lamp lights after brief pause.	NO DATA lamp, CP4
13	Operate and hold RESET switch.	Counter display reads 00.	CP1
		OVERFLOW lamp remains off.	
14	Release RESET switch.	Counter display counts. OVERFLOW lamp lights when count goes from 99 to 00.	OVERFLOW lamp.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
15	Rotate the BIT RATE switch through all positions (150 – 2400).	Counter display rate increases for each increasing BIT RATE switch position.	CP1, CP2
16	Set BIT RATE switch to EXT +.	Counter display stops.	
		NO CLOCK lamp lights after brief pause.	NO CLOCK lamp, CP4
17	Set BIT RATE switch to EXT –.	Counter display remains stopped. NO CLOCK lamp remains lighted. May go out momentarily. No clock and no data lamp.	
18	Set FUNCTION switch to VOLT/ OHM EXT.	NO CLOCK and NO DATA lamps.	
19	Set the TEST SET MODE switch to TRMT SER.	NO CLOCK lamp remains lighted. May go out momentarily.	
		NO DATA lamp remains lighted. May go out momentarily.	
20	Set the RANGE switch to DCV/1.	Meter indicates 0.7 ±0.1 dc volts.	CP4
		NOTE: If meter reads down-scale, set POLARITY switch to opposite position.	
21	Operate BIT RATE switch between EXT + and EXT – until proper meter indication is obtained.	Meter reads down-scale.	
22	Set the POLARITY switch to the opposite position.	Meter indicates 0.7 ±.1 dc volts.	CP4
23	Set RANGE switch to DCV/10.	Meter indicates 4.0 ±0.5 dc volts.	
24	Set the SIGNAL LEVEL switch to ±4V.		
25	Operate BIT RATE switch between EXT + and EXT – until proper meter indication is obtained.	Meter reads down-scale.	
26	Set the POLARITY switch to the opposite position.	Meter indicates 4.0 ±0.5 volts.	CP4
27	Set FUNCTION switch to OFF.		
28	Set SIGNAL LEVEL switch to ±.7V.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
29	Set BIT RATE switch to 1600.		
30	Set RANGE switch to ACV/1.		
31	Set FUNCTION switch to SPKR.	Raspy noise heard in loudspeaker.	
32	Rotate RANGE switch through all ACV positions.	Loudspeaker level increases as switch is rotated ccw.	
33	Operate POWER switch.	POWER lamp goes off.	
34	Remove test connections.		

6.08 **Parallel Data Circuits:** The following procedure tests the ability of the 1914B to generate the proper type of signals for parallel-data sets.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect a lead from the black INPUT terminal to TP1 and connect another lead from the red INPUT terminal to TP2.		
2	Connect the 4-dB pad between TP1 and TP2.		
3	Connect the interface cable between Connector A and Connector D, and connect the second cable between Connector B and Connector C.		
4	Set front-panel controls as follows: TEST MODE switch to ALL DOT. TEST SET MODE switch to TRMT 402. BIT RATE switch to EXT +. SIGNAL LEVEL switch to ±4V. FUNCTION switch to OFF. RANGE switch to ACV/1. WORD LENGTH switch to DOT.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
	COUNTER switch to BIT ERRORS.		
5	Insert shorting pins in the following matrix positions: row GRD, column 25. row TP2, column 25.		
6	Operate POWER switch.	POWER lamp lights.	
7	Set FUNCTION switch to VOLT/OHM EXT.		
8	Insert a shorting pin in matrix row TP1, column 2.	Meter indicates 0.7 to 1.1 volts ac.	CP5, CP8
9	Repeat Step 8 by removing pin from column 2 and inserting it in columns 3, 4, 5, 7, 8, 9, and 10 successively.	Meter indicates 0.7 to 1.1 volts ac.	CP5, CP8
10	Remove the shorting pin from matrix row TP1, column 10 and insert it in row TP1, column 6.	Meter indicates 0.5 to 0.75 volts ac.	CP5, CP8
11	Set the WORD LENGTH switch to 63.		
12	Set the TEST MODE switch to ALL RDM.		
13	Remove the shorting pin from matrix row TP1, column 6.		
14	Repeat Steps 8 and 9.	Meter indicates 0.4 to 0.9 volts ac. **NOTE:** Meter pointer "jitters" as result of random test messages.	CP5, CP8
15	Set TEST MODE switch to CHAN/1.		
16	Remove shorting pin from matrix row TP1 column 10, and insert it in row TP1, column 2.	Meter indicates 0.35 to 0.7 volts ac.	
17	Set TEST MODE switch to CHAN/2.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
18	Move the shorting pin in matrix row TP1 from column 2 to column 3.	Meter indicates 0.35 to 0.7 volts ac.	
19	Set TEST MODE switch to CHAN/3.		
20	Move the shorting pin in matrix row TP1 from column 3 to column 4.	Meter indicates 0.35 to 0.7 volts ac.	
21	Set TEST MODE switch to CHAN/4.		
22	Move the shorting pin in matrix row TP1 from column 4 to column 5.	Meter indicates 0.35 to 0.7 volts ac.	
23	Set TEST MODE switch to CHAN/5.		
24	Move the shorting pin in matrix row TP1 from column 5 to column 7.	Meter indicates 0.35 to 0.7 volts ac.	
25	Set TEST MODE switch to CHAN/6.		
26	Move the shorting pin in matrix row TP1 from column 7 to column 8.	Meter indicates 0.35 to 0.7 volts ac.	
27	Set TEST MODE switch to CHAN/7.		
28	Move the shorting pin in matrix row TP1 from column 8 to column 9.	Meter indicates 0.35 to 0.7 volts ac.	
29	Set TEST MODE switch to CHAN/8.		
30	Move the shorting pin in matrix row TP1 from column 9 to column 10.	Meter indicates 0.35 to 0.7 volts ac.	
31	Operate POWER switch.	POWER lamp goes off.	
32	Remove all test connections.		

6.09 Reference Voltage: The following procedure checks the seven fixed voltages and the adjustable voltage from the reference voltage supply.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Insert a shorting pin in matrix row TP3, column 1.		
2	Set OUTPUT switch to OFF.		
3	Operate POWER switch.	POWER lamp is lighted.	
4	Set FUNCTION switch to VOLT INT.		
5	Set RANGE switch to DCV/10.		
6	Set POLARITY switch to NOR.		
7	Set VERTICAL MONITOR switch to 1.		
8	Set ADJUST controls fully counterclockwise, both coarse (outer) and fine (inner).		
9	Set SELECT switch to ADJ.		
10	Set OUTPUT switch to TP3.	Meter indicates 0 dc volts.	
11	Rotate both coarse and fine ADJUST controls fully cw.	Meter pointer varies smoothly and indicates +10.0 ±0.5 dc volts with both controls fully cw.	
12	Rotate the fine (small) control fully ccw.	Meter indicates at least 0.5 volt dc less than value read in Step 11.	
13	Check each of the SELECT switch settings of Table B.	Meter indications shown in Table B.	
14	Operate POWER switch.	POWER lamp goes off.	
15	Remove test connections.		

Table B. Reference Voltages

RANGE SWITCH SETTING	POLARITY SWITCH SETTING	SELECT SWITCH SETTING	NORMAL METER INDICATION
DCV/3	REV	-2.0	1.90 to 2.10
DCV/1	REV	-1.0	0.95 to 1.05

Table B. Reference Voltages (Cont)

RANGE SWITCH SETTING	POLARITY SWITCH SETTING	SELECT SWITCH SETTING	NORMAL METER INDICATION
DCV/1	REV	-.477	0.45 to 0.50
DCV/1	———	0	0
DCV/1	NOR	+.477	0.45 to 0.50
DCV/1	NOR	+1.0	0.95 to 1.05
DCV/3	NOR	+2.0	1.90 to 2.10
DCV/10	NOR	+7.0	6.65 to 7.35

6.10 Clock Circuits: The following procedure uses an electronic counter to check the clock rates of the 1914B.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect leads from the CLOCK and GRD terminals of the 1914B to the appropriate input terminals of an electronic counter.		
2	Set front-panel controls as follows: TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS.		
3	Operate POWER switches on both 1914B and counter.	1914B POWER lamp is lighted and counter is turned on. **NOTE**: Allow the 1914B and counter to warm up for 5 minutes before proceeding.	
4	Set the BIT RATE switch to positions 150 through 2400.	Counter readings should be within the tolerances shown in the Table C.	CP1, CP2
5	Set the COUNTER switch to each of the four INTERVAL positions.	Counter readings should be within the tolerances shown in the Table D.	

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
6	Set the BIT RATE switch to EXT +.		
7	Set the COUNTER switch to BIT ERRORS.		
8	Set the TEST SET MODE switch to TRMT 402.	Counter should read 75 ± 4 Hz.	CP5
9	Operate the POWER switches at both the 1914B and counter.	POWER lamp goes off and counter is turned off.	

Table C. Bit Rate Test

BIT RATE SWITCH POSITION	ELECTRONIC COUNTER FREQUENCY (Hz)
150	150 ± 5
300	300 ± 9
600	600 ± 18
1,000	1,000 ± 30
1,200	1,200 ± 36
1,400	1,400 ± 42
1,600	1,600 ± 48
1,800	1,800 ± 54
2,000	2,000 ± 60
2,400	2,400 ± 72

Table D. Counter Test

COUNTER INTERVAL SWITCH POSITION	ELECTRONIC COUNTER FREQUENCY (Hz)
X .1	10,000 ± 250
X 1	1,000 ± 25
X 10	100 ± 3.0
X 100	10 ± 0.3

6.11 Data and Sample Circuits: In the following procedure, the data sync, and clock outputs of the 1914B are checked with the aid of a dual-trace oscilloscope. The dual traces permit checking the phase relationship of the data and clock signals. The oscilloscope must have a variable time base and must be capable of being externally synchronized.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect the oscilloscope to the 1914B as follows: Connect a lead from the CLOCK terminal of the 1914B to the channel 1 input of the oscilloscope. Connect a lead from the SYNC terminal of the 1914B to both the sync terminal and the channel 2 input of the oscilloscope.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
	Connect a lead from the GRD terminal of the 1914B to the ground terminal of the oscilloscope.		
2	Set the 1914B front-panel controls as follows: TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS. BIT RATE switch to 1000. SIGNAL LEVEL switch to ±4v. WORD LENGTH switch to 63. SAMPLE WIDTH switch to .5 μs.		
3	Operate the POWER switches on both the 1914B and the oscilloscope.	POWER lamp lights and the oscilloscope turns on.	
4	Set the oscilloscope controls to observe the channel 2 input using external sync on the oscilloscope.	Observe waveform A, Figure 15.	CP5, CP4
5	Set the oscilloscope controls to observe the channel 1 input using external sync on the oscilloscope.	Observe waveform B, Figure 15.	
6	Set the WORD LENGTH switch to 511.		
7	Set the oscilloscope controls to observe the channel 1 input first and then the channel 2 input.	Waveforms observed in Steps 4 and 5 do not change.	CP3
8	Remove the lead between the SYNC terminal and the oscilloscope channel 2 input.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
9	Connect a lead from the DATA OUT jack to the oscilloscope channel 2 input.		
10	Set the oscilloscope controls to observe channel 1 and 2 inputs simultaneously using external sync.	Observe waveform C, Figure 15.	
11	Set the WORD LENGTH switch to 63.	Observe waveform D, Figure 15.	CP3
12	Set the WORD LENGTH switch to DOT.	Using internal sync at the oscilloscope, observe waveform E, Figure 15.	CP3
13	Disconnect the oscilloscope lead from the CLOCK jack. With the ac power off, remove the test set case and reapply ac power. Connect the oscilloscope lead to test point TP1 of circuit pack CP2 (see Paragraph 6.03 and Figure 11).		
14	Remove the oscilloscope sync lead from the 1914B SYNC terminal and connect the lead to the CLOCK jack.		
15	Using external sync, set the oscilloscope controls to adjust time base so that one bit interval of the data signal occupies a 10-cm sweep on the graticule.	On channel 1 of the oscilloscope, observe a very narrow positive pulse at center of display.	CP3
16	Turn the SAMPLE WIDTH switch to each of its % positions (10% through 50%).	Observe on the oscilloscope screen that the pulse width of the channel 1 input is within ±4% of the value marked on each SAMPLE WIDTH switch position. Each pulse is centered within 2% along the vertical axis of the oscilloscope.	
17	Operate both the 1914B and oscilloscope POWER switches.	POWER lamp is turned off and the oscilloscope is turned off.	
18	Remove test connections. Unplug unit and mount it back in its case.		

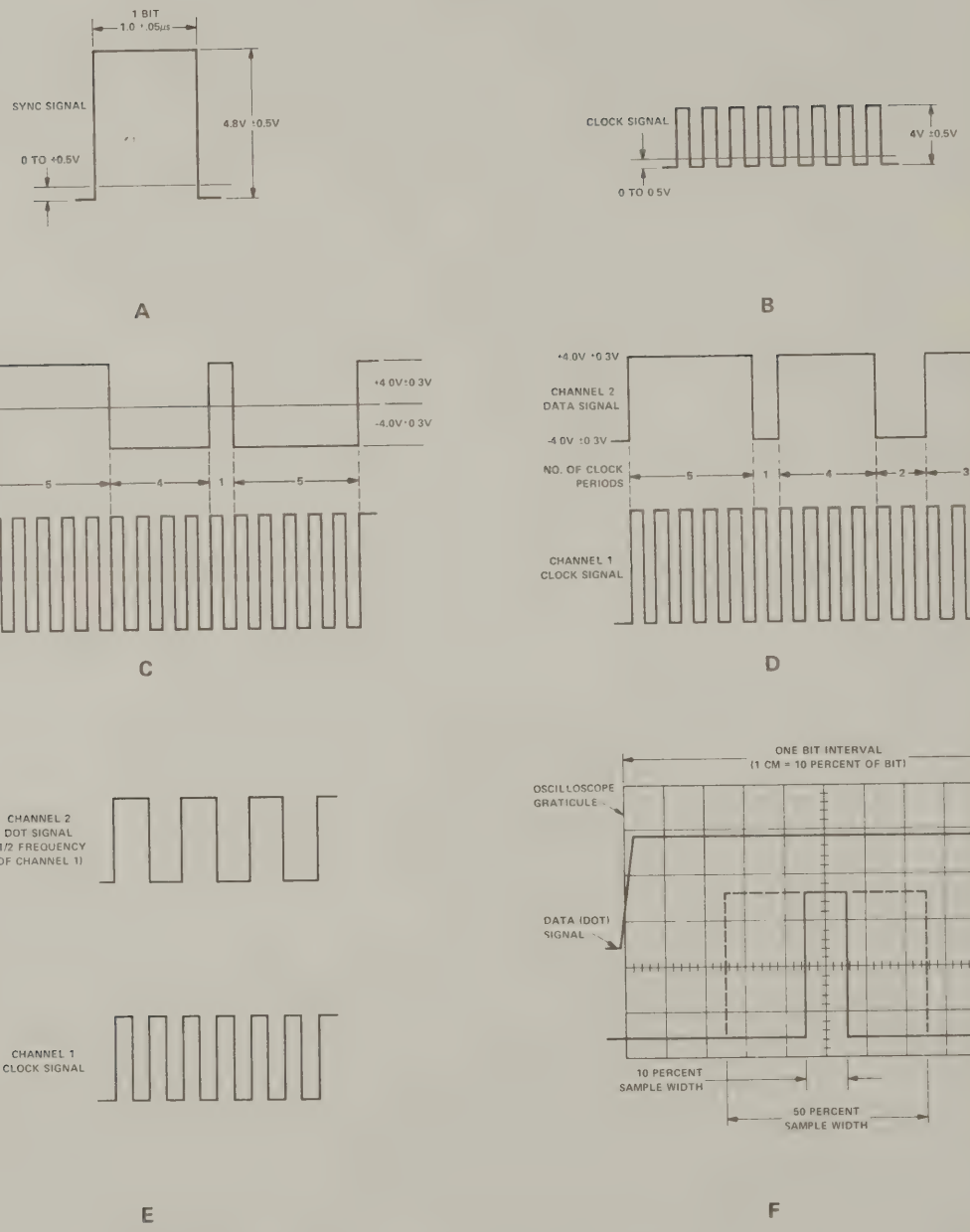


Figure 15. Data and Sample Circuit Waveforms

6.12 **AC Voltmeter**: The following procedure permits calibrating the ac voltmeter with the aid of an external reference signal of preferably 0 dBm level known to be accurate to within 0.1 dB.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect the output of the reference generator to the INPUT terminals of the 1914B.		
2	Turn on the signal generator and set its output to some known value within the ac volts range of the 1914B meter.		
3	Operate the 1914B POWER switch.		
4	Turn the 1914B FUNCTION switch to VOLT/OHM EXT.		
5	Set the 1914B RANGE switch to the highest ac range that will permit the nearest full-scale meter deflection.		
6	If the meter reading is not the same as the known input voltage, remove the rear cover of the 1914B as described in Paragraph 6.03 and adjust R17 (Figure 11) until the meter reading agrees with the known voltage.		
7	Remove test connections.		
8	Turn power off.		

Tests on Two Interconnected 1914B's

6.13 The tests of Paragraphs 6.14 and 6.15 use two 1914B test sets so interconnected that one serves as the transmitter and the other the receiver.

6.14 Word Generator, Clock, and Sync Circuits: The following procedure checks the data and clock circuits of one 1914B as a transmitter (Set A) and another 1914B as a receiver (Set B).

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect the interface cable from Connector A on Set A (transmitter) to Connector A on Set B (receiver).		
2	On the front panel of Set A, set the controls as follows: TEST SET MODE switch to TRMT SER. COUNTER switch to BIT ERRORS.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
	BIT RATE switch to 150. SIGNAL LEVEL switch to ±4V. WORD LENGTH switch to 63.		
3	In the matrix of Set A, insert a shorting pin in the following position: row GRD, column 1		
4	On the front panel of Set B, set the controls as follows: TEST SET MODE switch to RCV SER. COUNTER switch to BIT ERRORS. FUNCTION switch to PHASE ADJ. BIT RATE switch to 150. SIGNAL LEVEL switch to ±4V. WORD LENGTH switch to 63. SAMPLE WIDTH switch to .5 μs. WORD SYNC switch to OFF.		
5	In the matrix of Set B, insert shorting pin in the following positions: row GRD, column 1 row RD, column 2		
6	Operate the POWER switches on both sets.	POWER lamps light.	

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
7	In the matrix of Set A, insert a shorting pin in row SD, column 2.	Set B meter pointer deflects. The NO DATA and NO CLOCK lamps go off. Counter display starts.	CP1, CP2, CP3, CP4
8	Adjust the Set B PHASE control.	Set B meter pointer nulls to zero.	CP1, CP2, CP3, CP4
9	Turn the Set B FUNCTION switch to OFF.		
10	Momentarily operate the Set B WORD SYNC switch to MAN.	Set B counter display stops.	
11	Turn the Set A WORD LENGTH switch to 511, then return to 63.	Set B counter display starts	
12	Set the Set B WORD SYNC switch to AUTO.	Set B counter display stops.	
13	Depress RESET button.	Display shows 00, OVERFLOW lamp is off.	
14	Set the WORD LENGTH switches on both test sets to 511.	Set B counter display may run momentarily, then stop.	CP3
15	Set the BIT RATE switches of both test sets to 300.		
16	Set the Set B FUNCTION switch to PHASE ADJ.		
17	Adjust the Set B PHASE control for zero indication.	Meter pointer indicates zero.	
18	Set the Set B FUNCTION switch to OFF.	Counter display may run momentarily, then stop.	
19	Repeat Steps 15 through 18 for each BIT RATE switch position through 2400.	Same as in Steps 15 through 18.	
20	Set the Set B WORD SYNC switch to OFF.		
21	Set the Set A WORD LENGTH switch to 63.		
22	Set the Set B COUNTER switch to BLOCK ERRORS/WL.	The Set B counter display runs at a slower rate.	CP5, CP8

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
23	Turn the Set B COUNTER switch to each BLOCK ERROR position through 16 WL.	The counter display runs at a decreasing rate for each increase in block length.	CP5, CP8
24	Operate the POWER switches of both test sets.	POWER lamps are turned off.	
25	Remove all test connections.		
	NOTE: The two 1914B's should now be exchanged and the above tests rerun so that the transmitting and receiving functions of both sets will be tested.		

6.15 Parallel Data Circuits: The following procedure tests the parallel-data mode in both the transmitting and receiving test sets.

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
1	Connect a test cable from Connector C on Set A (transmitter) to Connector D on Set B (receiver).		
2	On the front panel of Set A, set the controls as follows: TEST MODE switch to ALL RDM. WORD LENGTH switch to 63. TRMTR CLOCK PHASE switch to ADV. SIGNAL LEVEL switch to ±4V. TEST SET MODE switch to TRMT 402. COUNTER switch to BIT ERRORS. BIT RATE switch to EXT +.		
3	On the front panel of Set B, set the controls as follows: TEST MODE switch to ALL RDM.		

STEP	PROCEDURE	NORMAL INDICATION	POSSIBLE CAUSE OF ABNORMAL CONDITION
	TEST SET MODE switch to RCV 402. WORD LENGTH switch to 63. SIGNAL LEVEL switch to ±4V. TRMTR CLOCK PHASE switch to NOR. COUNTER switch to BIT ERRORS. BIT RATE switch to EXT -. WORD SYNC switch to OFF.		
4	Operate the POWER switches on both test sets.	POWER lamps light. Set B counter display runs.	
5	Momentarily operate set B WORD SYNC switch to MAN.	Set B counter display stops.	
6	Set TEST MODE switches on both sets to CHAN 1.	Set B counter display may run.	
7	Momentarily operate Set B WORD SYNC switch to MAN.	Set B counter display stops.	
8	Repeat Steps 6 and 7 for TEST MODE/CHAN switch positions 2 through 8.	Same as Steps 6 and 7.	
9	Operate POWER switches on both test sets.	POWER lamps go off.	
10	Remove all test connections. NOTE: The two 1914B's should now be exchanged and the above tests rerun so that the transmitting and receiving functions of both sets will be tested.		

7. REFERENCES

7.01 Additional information on the Model 1914B can be obtained from the following source: Sierra 1914B Data Transmission Test Set Maintenance Manual SMM-1914B.

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Warranty

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This warranty does not apply to any products which have been repaired, worked upon or altered by persons not authorized by us so as, in our sole judgement, to injure the stability or reliability of such instrument, or which have been subject to misuse, negligence or accident, or the serial number of which has been altered, effaced, or removed. Neither does this warranty apply to any of our products which have been connected, installed, used or adjusted otherwise than in accordance with the instructions furnished by us. Nor does SIERRA assume any liability for consequential damages, and in any event our liability shall in no case exceed the original purchase price of the instrument. Accessories, including but not limited to all vacuum tubes, fuses and batteries, not of our manufacture used with this product are not covered by this warranty.

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